ABSTRACT OF THE DISCLOSURE

A processing system has a processor core (104) executing instructions of a first instruction set and an instruction translator (108) for generating translator output signals corresponding to one or more instructions of the first instruction set so as to emulate instructions of a second instruction set. The instruction translator (108) provides translator output signals specifying operations that are arranged so that the input variables to an instruction of the second instruction set are not changed until the final operation emulating that instruction is executed. An interrupt handler services an interrupt after execution of an operation of the instructions of the first instruction set. Arranging the translated sequences of instructions such that the input state is not altered until the final instruction is executed has the result that processing may be restarted after the interrupt either by rerunning the complete emulation if the final operation had not started when the interrupt occurred, or by running the next instruction from the second instruction set if the final operation had started when the interrupt occurred.

[Figure 8]